Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-8. (Canceled)

9. (Original) A method for fabricating a semiconductor package, comprising:

forming a plated copper pattern formed plate by:

forming a first plated copper layer on upper and lower surfaces of a first insulation substrate;

forming a pattern on first plated copper formed at the upper and lower surfaces of the first insulation substrate; and

forming an opening by removing a central portion of the first insulation substrate with the first plated copper pattern formed thereon;

forming an inner circuit pattern formed plate by:

forming a second plated copper pattern on an upper surface or a lower surface of a second insulation substrate;

forming a third plated copper layer on a second plated copper; and

forming an opening by removing a central portion of the second insulation substrate with the second plated copper pattern and the third plated copper formed thereon;

forming a lower circuit pattern formed by:

forming a fourth plated copper pattern on an upper surface or a lower surface of a third insulation substrate;

forming a fifth plated copper layer on the fourth plated copper;

forming an opening by removing a central portion of the third insulation substrate with the fourth plated copper pattern and the fifth plated copper formed thereon;

forming a bonding pad by forming a first nickel/gold plating layer around the opening of the inner circuit pattern formed plate and the lower circuit pattern formed plate;

forming a laminated body by laminating the plated copper pattern formed plate onto the inner circuit pattern formed plate and the inner circuit pattern formed plate onto the lower circuit pattern formed plate using bonding sheets and sequentially attaching the formed plates;

forming a through bore in the laminated body;

forming a sixth plated copper layer on an inner circumferential surface of the through bore, the surface of the laminated body and the first nickel/gold plating layer;

removing the sixth plated copper layer formed on the first nickel/gold plating layer of the laminated body;

forming an outer circuit pattern by patterning a plated copper formed with the sixth plated copper layer formed thereon; and

forming a second nickel/gold plating layer on the first nickel/gold plating layer of the laminated body and at a predetermined portion of the outer circuit pattern formed at an upper surface of the laminated body to form a bonding pad and a ball pad, respectively.

10. (Original) The method of claim 9, wherein the insulation substrate is formed of one of glass epoxy, glass polyimide and a bismaleimide triazine resin.

11. (Original) The method of claim 9, wherein the first nickel/gold plating layer is formed by an electroless nickel/gold plating, wherein a nickel plating layer is formed, and a gold plating layer is formed at an upper surface of the nickel plating layer.

12. (Original) The method of claim 11, wherein the nickel plating layer is formed with a thickness of less than about 0.7μm and the gold plating layer is formed with a thickness of below about 0.3μm, wherein the first nickel/gold plating layer has a thickness of below about 1μm.

13. (Original) The method of claim 9, wherein the openings of the plated copper pattern formed plates are larger than the openings of the inner circuit pattern formed plates and

the openings of the inner circuit pattern formed plates are larger that the openings of the circuit pattern formed plates.

14. (Original) The method of claim 9, wherein the bonding sheets are formed of prepreg sheets, which are formed by setting glass fibers in an adhesive.

15. (Original) The method of claim 9, wherein the through hole is filled with a filler comprising a conductive paste or a resin material.

16. (Original) The method of claim 9, further comprising:

attaching a solder ball to the ball pad formed at the upper surface of the laminated body, and attaching a heat sink to a lower surface of the laminated body.

17-19. (Canceled)

20. (Currently Amended) A method of forming a semiconductor package, comprising:

forming a plurality of plates, wherein each plate is formed by:

~~coating~~ forming a first coating on a substrate; and

forming an opening in a central portion of the substrate with the first coating thereon;

forming a bonding pad pattern on at least one of the plurality of plates, wherein a second coating is coated onto the bonding pad pattern;

forming a body by stacking the plurality of plates;

forming a through bore in the body; and

coating the through bore with a third coating.

21. (Original) The method of claim 20, wherein the second coating comprises a non-copper metal coating and is applied to the bonding pad pattern, wherein the bonding pad pattern is formed around the opening on at least a vertical surface of the opening of at least one of the plurality of plates.

22. (Original) The method of claim 21, wherein the second coating comprises Ni-Au.

23. (Original) The method of claim 20, wherein the first and third coatings comprises copper.

24. (Original) The method of claim 20, further comprising mounting a semiconductor chip to the body by:

forming a heat sink along a bottom surface of the body;

mounting the semiconductor chip to the heat sink; and

connecting the semiconductor chip to the second coating and the bonding pad.

25. (Original) The method of claim 20, wherein the plurality of plates comprise three plates.

26. (Original) The method of claim 25, wherein the three plates comprise:

an upper plate;

an inner circuit plate formed on a lower surface of the upper plate; and

a lower circuit pattern plate formed on a lower surface of the inner circuit plate, wherein the opening in the upper plate is larger than the opening in the inner circuit plate and the opening in the inner circuit plate is larger than the opening in the lower circuit plate.

27. (Original) The method of claim 20, wherein the forming of the body further comprises inserting laminating sheets between the plurality of plates to bond the plates together and form the body.

28. (Original) The method of claim 27, wherein the laminating sheets comprise fibers in an adhesive.

29. (Original) The method of claim 26, wherein the bonding pad pattern is formed on at least a vertical surface of the opening of at least one of the plurality of plates.

30. (Original) The method of claim 29, wherein the second coating on the bonding pad pattern comprises Ni-Au.

31. (Original) The method of claim 26, wherein the first and third coatings comprises copper.

32. (Original) The method of claim 20, further comprising:

coating a fourth coating on the second coating, wherein the fourth coating is coated thicker than the second coating, and wherein the second and the fourth coatings comprise Ni-Au coatings.

33. (Currently Amended) The method of claim 20, wherein the substrate comprises:

glass epoxy;

glass polyimide; or

bismaleimide triazine (BT).

34-35. (Canceled)

36. (New) A method for manufacturing a printed circuit board, comprising:

forming a circuit pattern on each of a plurality of plates;

forming an opening in each of the plurality of said plates so as to define cavities having different sizes;

forming a bonding pad pattern on at least one of the plurality of plates, wherein a second coating is coated onto the bonding pad pattern;

forming a body by stacking the plurality of plates so as to form a multi-step cavity in said body;

forming a through bore in the body and coating a third coating therein; and

removing said third coating on said bonding pad pattern.

37. (New) The method of claim 35, further comprising:

forming a fourth coating on said bonding pad pattern.

38. (New) The method for claim 37, wherein said fourth coating is coated thicker than said second coating, and wherein said second and the fourth coatings comprise Ni-Au coatings.

39. (New) The method of claim 35, wherein said second coating comprises a non-copper metal coating and is applied to said bonding pad pattern.

40. (New) The method of claim 35, wherein said second and/or said fourth coatings comprises Ni-Au.

41. (New) The method of claim 35, wherein said third coating comprises copper.

42. (New) The method of claim 35, further comprising mounting a semiconductor chip to the body by:

forming a heat sink along a bottom surface of the body;

mounting the semiconductor chip to the heat sink; and

connecting the semiconductor chip to the second coating and the bonding pad.